## CLAIMS

WHAT IS CLAIMED:

1. A method for patterning a process layer in a semiconductor device, comprising:

forming the process layer above a structure layer;

forming a cap layer above the process layer;

forming a photoresist layer above the cap layer;

forming an opening in the photoresist layer;

performing a first anisotropic etch into a region of the cap layer underlying the opening in the photoresist layer to form an etched region in the cap layer, leaving a portion of the cap layer in the etched region;

removing the photoresist layer from above the cap layer; and

performing a second anisotropic etch to form an etch pattern in the process layer.

2. The method of claim 1, wherein forming the process layer above a structure layer comprises forming a dielectric layer above a structure layer.

3. The method of claim 2, wherein forming a dielectric layer above a structure layer comprises depositing a dielectric layer above a structure layer.

4. The method of claim 3, wherein depositing a dielectric layer above a structure layer comprises depositing a dielectric layer of a material having a dielectric constant less than approximately 4 above a structure layer.

5. The method of claim 1, wherein forming a cap layer above the process layer comprises depositing a cap layer of at least one of TEOS oxide, silicon nitride and silicon carbide above the process layer.

6. The method of claim 1, further comprising forming an anti-reflective coating layer above the cap layer before forming a photoresist layer above the cap layer.

7. The method of claim 6, wherein performing a first anisotropic etch into a region of the cap layer underlying the opening in the photoresist layer comprises performing a first anisotropic etch through a region of the anti-reflective coating layer underlying the opening in the photoresist layer and into a region of the cap layer underlying the opening in the photoresist layer.

8. The method of claim 7, further comprising removing all of the anti-reflective coating layer and at least substantially all of the cap layer while performing the second anisotropic etch.

9. The method of claim 7, further comprising removing the anti-reflective coating layer and the cap layer.

10. The method of claim 7, further comprising:

removing a portion of the anti-reflective coating layer while performing the second anisotropic etch; and

thereafter, removing a remaining portion of the anti-reflective coating layer and removing at least substantially all of the cap layer.

11. The method of claim 10, wherein removing a remaining portion of the anti-reflective coating layer and removing at least substantially all of the cap layer comprises removing a remaining portion of the anti-reflective coating layer by a chemical mechanical polishing process and removing at least substantially all of the cap layer by a chemical mechanical polishing process.

12. The method of claim 6, wherein forming an anti-reflective coating layer above the cap layer comprises forming an anti-reflective coating layer of at least one of silicon nitride, silicon oxynitride and silicon carbide above the cap layer.

13. The method of claim 12, wherein forming a cap layer above the process layer comprises forming a cap layer of at least one of TEOS oxide, silicon nitride and silicon carbide above the process layer.

14. The method of claim 1, wherein removing the photoresist layer from above the cap layer comprises ashing the photoresist layer from above the cap layer.

15. The method of claim 1, wherein performing a first anisotropic etch into a region of the cap layer underlying the opening in the photoresist layer comprises performing a first anisotropic etch by one of plasma etching and wet chemical etch into a region of the cap layer underlying the opening in the photoresist layer.

16. The method of claim 1, wherein performing a second anisotropic etch to form an etch pattern in the process layer comprises performing a second anisotropic etch by one of plasma etching and wet chemical etch to form an etch pattern in the process layer.

17. The method of claim 1, further comprising removing at least substantially all of the cap layer while performing the second anisotropic etch.

18. The method of claim 1, further comprising:

thinning the cap layer while performing the second anisotropic etch; and

thereafter, removing a remaining portion of the cap layer.

19. The method of claim 18, wherein removing a remaining portion of the cap layer comprises removing a remaining portion of the cap layer by a chemical mechanical polishing process.

20. The method of claim 1, further comprising removing the cap layer.

21. The method of claim 1, wherein the structure layer comprises a semiconductor substrate.

22. The method of claim 1, wherein the structure layer comprises a layer of conductive material.

23. The method of claim 22, wherein the layer of conductive material comprises a patterned layer of conductive material.

24. A method for forming a conductive interconnect in a semiconductor device, comprising:

forming a dielectric layer above a structure layer;

forming a cap layer above the dielectric layer;

forming a photoresist layer above the cap layer;

forming an opening in the photoresist layer;

performing a first anisotropic etch into a region of the cap layer underlying the opening in the photoresist layer to form an etched region in the cap layer, leaving a portion of the cap layer in the etched region;

removing the photoresist layer from above the cap layer;

performing a second anisotropic etch to form an opening in the dielectric layer, the opening in the dielectric layer having a sidewall;

forming a barrier layer above at least the sidewall of the opening in the dielectric layer;

forming a conductive material in at least the opening in the dielectric layer; and

removing the cap layer.

25. The method of claim 24, wherein forming a dielectric layer above a structure layer comprises depositing a dielectric layer above a structure layer.

26. The method of claim 25, wherein depositing a dielectric layer above a structure layer comprises depositing a dielectric layer of a material having a dielectric constant less than approximately 4 above a structure layer.

27. The method of claim 25, wherein depositing a dielectric layer above a structure layer comprises depositing a dielectric layer of silicon dioxide above a structure layer.

28. The method of claim 25, wherein depositing a dielectric layer above a structure layer comprises depositing a dielectric layer of a material having a dielectric constant less than about 4.0 above a structure layer.

29. The method of claim 24, wherein forming a cap layer above the dielectric layer comprises depositing a cap layer of at least one of TEOS oxide, silicon nitride and silicon carbide above the dielectric layer.

30. The method of claim 24, wherein removing the photoresist layer from above the cap layer comprises ashing the photoresist layer from above the cap layer.

31. The method of claim 24, wherein performing a first anisotropic etch into a region of the cap layer underlying the opening in the photoresist layer comprises performing a first anisotropic etch by one of plasma etch and wet chemical etch into a region of the cap layer underlying the opening in the photoresist layer.

32. The method of claim 24, wherein performing a second anisotropic etch to form an opening in the dielectric layer comprises performing a second anisotropic etch by one of plasma etch and wet chemical etch to form an opening in the dielectric layer.

33. The method of claim 24, wherein forming a barrier layer above at least the sidewall of the opening in the dielectric layer comprises forming a layer of at least one of

tantalum, tantalum nitride and titanium nitride above at least the sidewalls of the opening in the dielectric layer.

34. The method of claim 24, wherein forming a barrier layer above at least the sidewall of the opening in the dielectric layer comprises forming a layer of at least one of titanium-tungsten, nitrided titanium-tungsten, and magnesium above at least the sidewall of the opening in the dielectric layer.

35. The method of claim 24, wherein forming a conductive material in at least the opening in the dielectric layer comprises forming a conductive material of copper in at least the opening in the dielectric layer.

36. The method of claim 24, wherein removing the cap layer comprises removing the cap layer by a chemical mechanical polishing process.

37. The method of claim 24, wherein performing a second anisotropic etch to form an opening in the dielectric layer comprises performing a second anisotropic etch to form an opening in the dielectric layer and to thin the cap layer.

38. The method of claim 37, wherein removing the cap layer comprises removing a remaining portion of the cap layer.

39. The method of claim 24, wherein forming a conductive material in at least the opening in the dielectric layer comprises:

depositing a copper seed layer above the barrier layer; and

forming copper material in the opening using an electroplating process.

40. The method of claim 39, further comprising performing a chemical mechanical polishing process to remove an excess of copper.

41. The method of claim 40, wherein removing the cap layer comprises removing the cap layer by a chemical mechanical polishing process.

42. The method of claim 24, wherein the structure layer comprises a semiconductor substrate.

43. The method of claim 24, wherein the structure layer comprises a layer of conductive material.

44. The method of claim 43, wherein the layer of conductive material comprises a patterned layer of conductive material.

45. A method for forming a conductive interconnect in a semiconductor device, comprising:

forming a first process layer above a semiconductor substrate;

forming a second process layer above the first process layer;

forming a mask above the second process layer, the mask having an opening therein;

performing a first anisotropic etch into a region of the second process layer underlying the opening in the mask;

removing the mask from above the second process layer;

performing a second anisotropic etch to form an opening in the first process layer; and forming a conductive material in the opening in the first process layer.

46. The method of claim 45, wherein forming a first process layer comprises forming a first process layer of a dielectric material.

47. The method of claim 46, wherein the dielectric material comprises a dielectric material having a dielectric constant less than approximately 4.

48. The method of claim 46, wherein the dielectric material comprises at least one of silicon dioxide, and a material having a dielectric constant of less than about 4.0.

49. The method of claim 45, wherein forming a second process layer above the first process layer comprises forming a cap layer above the first process layer.

50. The method of claim 49, wherein forming a cap layer above the first process layer comprises forming a layer of at least one of TEOS oxide, silicon nitride and silicon carbide above the first process layer.

51. The method of claim 45, wherein forming a mask above the second process layer comprises forming a mask above the second process layer using a photoresist material.

52. The method of claim 51, wherein removing the mask from above the second process layer comprises ashing the photoresist material from above the second process layer.

53. The method of claim 45, wherein performing a second anisotropic etch to form an opening in the first process layer comprises performing a second anisotropic etch to form an opening in the first process layer and to thin the second process layer.

54. The method of claim 45, wherein performing a second anisotropic etch to form an opening in the first process layer comprises performing a second anisotropic etch to form an opening in the first process layer and to remove at least substantially all of the second process layer from above the first process layer.

55. The method of claim 45, wherein forming a conductive material in the opening in the first process layer comprises forming a conductive material of copper in the opening in the first process layer.

56. The method of claim 45, further comprising depositing a copper seed layer in at least the opening in the first process layer before forming a conductive material.

57. The method of claim 56, wherein forming a conductive material in the opening in the first process layer comprises forming a conductive material of copper in the opening in the first process layer by using an electroplating process.

58. The method of claim 45, further comprising forming a barrier layer in at least the opening in the first process layer before forming a conductive material in the opening in the first process layer.

59. A method for patterning a process layer in a semiconductor device, comprising:

forming a process layer above a structure layer;

forming a cap layer above the process layer;

forming a first photoresist layer above the cap layer;

forming a first opening in the first photoresist layer;

performing a first anisotropic etching process into a region of the cap layer underlying the first opening in the first photoresist layer to form an etched region in the cap layer, leaving a portion of the cap layer in the etched region;

removing the first photoresist layer from above the cap layer;

forming a second photoresist layer above the cap layer;

forming a second opening in the second photoresist layer;

performing a second anisotropic etching process into a region of the cap layer underlying the second opening in the second photoresist layer to enlarge the etched region in the cap layer, leaving a second portion of the cap layer in the etched region;

removing the second photoresist layer from above the cap layer; and

performing a third anisotropic etching process to form an etched pattern in the process layer.

60. The method of claim 59, wherein forming a process layer above the structure layer comprises forming a dielectric layer above the structure layer.

61. The method of claim 60, wherein forming a dielectric layer above the structure layer comprises depositing a dielectric layer above the structure layer.

62. The method of claim 61, wherein depositing a dielectric layer above the structure layer comprises depositing a dielectric layer of a material having a dielectric constant less than approximately 4 above the structure layer.

63. The method of claim 59, wherein forming a cap layer above the process layer comprises depositing a cap layer of at least one of TEOS oxide, silicon nitride and silicon carbide above the process layer.

64. The method of claim 59, further comprising forming an anti-reflective coating layer above the cap layer before forming the first photoresist layer above the cap layer.

65. The method of claim 64, wherein performing a first anisotropic etching process into a region of the cap layer underlying the first opening in the first photoresist layer comprises performing a first anisotropic etching process through a region of the anti-reflective coating layer underlying the first opening in the first photoresist layer and into a region of the cap layer underlying the first opening in the first photoresist layer.

66. The method of claim 65, further comprising removing all of the anti-reflective coating layer and at least substantially all of the cap layer while performing the third anisotropic etching process.

67. The method of claim 65, further comprising removing the anti-reflective coating layer and the cap layer.

68. The method of claim 67, wherein removing the anti-reflective coating and the cap layer comprises removing the anti-reflective coating layer and the cap layer by a chemical mechanical polishing process.

69. The method of claim 64, wherein forming an anti-reflective coating layer above the cap layer comprises forming an anti-reflective coating layer of at least one of silicon nitride, silicon oxynitride and silicon carbide above the cap layer.

70. The method of claim 59, wherein removing the first photoresist layer from above the cap layer comprises ashing the first photoresist layer from above the cap layer.

71. The method of claim 70, wherein removing the second photoresist layer from above the cap layer comprises ashing the second photoresist layer from above the cap layer.

72. The method of claim 59, wherein removing the second photoresist layer from above the cap layer comprises ashing the second photoresist layer from above the cap layer.

73. The method of claim 59, further comprising removing at least substantially all of the cap layer while performing the third anisotropic etching process.

74. The method of claim 59, further comprising:

thinning the cap layer while performing the third anisotropic etching process; and

thereafter, removing a remaining portion of the cap layer.

75. The method of claim 74, wherein removing a remaining portion of the cap layer comprises removing a remaining portion of the cap layer by a chemical mechanical polishing process.

76. The method of claim 59, wherein the structure layer comprises a semiconductor substrate.

77. The method of claim 59, wherein the structure layer comprises a layer of conductive material.

78. A method for patterning a process layer in a semiconductor device, comprising:

forming a process layer above a structure layer;

forming a first cap layer above the process layer;

forming a second cap layer above the first cap layer;

forming a first photoresist layer above the second cap layer;

forming a first opening in the first photoresist layer;

performing a first anisotropic etching process into a region of the second cap layer underlying the first opening in the first photoresist layer to form an etched region in the second cap layer;

removing the first photoresist layer from above the second cap layer;

forming a second photoresist layer above the second cap layer;

forming a second opening in the second photoresist layer, the second opening in the second photoresist layer overlying the etched region in the second cap layer;

performing a second anisotropic etching process into a region of the second cap layer underlying the second opening in the second photoresist layer and into a region of the first cap layer underlying the second opening in the second photoresist layer to form a second etched region in the first and second cap layers, leaving at least a portion of the first cap layer in the second etched region;

removing the second photoresist layer from above the second cap layer; and

performing a third anisotropic etching process to form an etched pattern in the process layer.

79. The method of claim 78, wherein forming a process layer above a structure layer comprises forming a dielectric layer above a structure layer.

80. The method of claim 79, wherein forming a dielectric layer above a structure layer comprises depositing a dielectric layer above a structure layer.

81. The method of claim 80, wherein depositing a dielectric layer above a structure layer comprises depositing a dielectric layer of a material having a dielectric constant less than approximately 4 above a structure layer.

82. The method of claim 78, wherein forming a first cap layer above the process layer comprises depositing a first cap layer of at least one of TEOS oxide, silicon nitride and silicon carbide above the process layer.

83. The method of claim 78, wherein forming a second cap layer above the first cap layer comprises depositing a second cap layer of at least one of TEOS oxide, silicon nitride and silicon carbide above the first cap layer.

84. The method of claim 78, further comprising forming an anti-reflective coating layer above the second cap layer before forming the first photoresist layer above the second cap layer.

85. The method of claim 84, wherein performing a first anisotropic etching process into a region of the second cap layer underlying the first opening in the first photoresist layer comprises performing a first anisotropic etching process through a region of the anti-reflective coating layer underlying the first opening in the first photoresist layer and into a region of the second cap layer underlying the first opening in the first photoresist layer.

86. The method of claim 85, further comprising removing all of the anti-reflective coating layer and at least substantially all of the second cap layer while performing the third anisotropic etching process.

87. The method of claim 85, further comprising removing all of the anti-reflective coating layer, all of the second cap layer, and at least substantially all of the first cap layer while performing the third anisotropic etching process.

88. The method of claim 85, further comprising removing the anti-reflective coating layer, the second cap layer and the first cap layer.

89. The method of claim 84, wherein forming an anti-reflective coating layer above the second cap layer comprises forming an anti-reflective coating layer of at least one silicon nitride, silicon oxynitride and silicon carbide above the second cap layer.

90. The method of claim 89, wherein forming a first cap layer above the process layer comprises forming a first cap layer of at least one of TEOS oxide, silicon nitride and silicon carbide above the process layer.

91. The method of claim 89, wherein forming a second cap layer above the first cap layer comprises forming a second cap layer of at least one of TEOS oxide, silicon nitride and silicon carbide above the first cap layer.

92. The method of claim 78, wherein removing the first photoresist layer from above the second cap layer comprises ashing the first photoresist layer from above the second cap layer.

93. The method of claim 78, wherein removing the second photoresist layer from above the second cap layer comprises ashing the second photoresist layer from above the second cap layer.

94. The method of claim 78, further comprising removing at least substantially all of the first cap layer while performing the third anisotropic etching process.

95. The method of claim 78, further comprising removing at least substantially all of the second cap layer while performing the third anisotropic etching process.

96. The method of claim 78, further comprising:

thinning the first cap layer while performing the third anisotropic etching process; and

thereafter, removing a remaining portion of the first cap layer.

97. The method of claim 96, wherein removing a remaining portion of the first cap layer comprises removing a remaining portion of the first cap layer by a chemical mechanical polishing process.

98. The method of claim 78, wherein the structure layer comprises a semiconductor substrate.

99. The method of claim 78, wherein the structure layer comprises a layer of conductive material.

100. The method of claim 99, wherein the layer of conductive material comprises a patterned layer of conductive material.

101. A method for patterning first and second process layers in a semiconductor device, comprising:

forming a first process layer above a structure layer;

forming a hard mask layer above the first process layer, the hard mask layer having an opening therein;

forming a second process layer above the hard mask layer and above the opening in the hard mask layer;

forming a cap layer above the second process layer;

forming a photoresist layer above the cap layer;

forming an opening in the photoresist layer;

performing a first anisotropic etching process into a region of the cap layer underlying the opening in the photoresist layer to form an etched region in the cap layer, leaving a portion of the cap layer in the etched region;

removing the photoresist layer from above the cap layer; and

performing a second anisotropic etching process to extend at least a portion of the etched region in the cap layer to a surface of the structure layer.

102. The method of claim 101, wherein forming the first process layer above a structure layer comprises forming a first dielectric layer above a structure layer.

103. The method of claim 101, wherein forming a second process layer above the hard mask layer and above the opening in the hard mask layer comprises forming a second dielectric layer above the hard mask layer and above the opening in the hard mask layer.

104. The method of claim 102, wherein forming a first dielectric layer above the structure layer comprises depositing a first dielectric layer above the structure layer.

105. The method of claim 103, wherein forming a second dielectric layer comprises depositing a second dielectric layer.

106. The method of claim 104, wherein depositing a first dielectric layer comprises depositing a first dielectric layer of a material having a dielectric constant less than approximately 4.

107. The method of claim 105, wherein depositing a second dielectric layer comprises depositing a second dielectric layer of a material having a dielectric constant less than approximately 4.

108. The method of claim 101, wherein forming a cap layer above the second process layer comprises depositing a cap layer of at least one of TEOS oxide, silicon nitride and silicon carbide above the second process layer.

109. The method of claim 101, further comprising forming an anti-reflective coating layer above the cap layer before forming a photoresist layer above the cap layer.

110. The method of claim 109, wherein performing a first anisotropic etching process into a region of the cap layer underlying the opening in the photoresist layer comprises performing a first anisotropic etching process through a region of the anti-reflective coating layer underlying the opening in the photoresist layer and into a region of the cap layer underlying the opening in the photoresist layer.

111. The method of claim 110, further comprising removing all of the anti-reflective coating layer and at least substantially all of the cap layer while performing the second anisotropic etching process.

112. The method of claim 110, further comprising:

removing a portion of the anti-reflective coating layer while performing the second anisotropic etching process; and

thereafter, removing a remaining portion of the anti-reflective coating layer and removing at least substantially all of the cap layer.

113. The method of claim 109, wherein forming an anti-reflective coating layer above the cap layer comprises forming an anti-reflective coating layer of at least one of silicon nitride, silicon oxynitride and silicon carbide above the cap layer.

114. The method of claim 113, wherein forming a cap layer above the second process layer comprises forming a cap layer of at least one of TEOS oxide, silicon nitride and silicon carbide above the second process layer.

115. The method of claim 101, wherein removing the photoresist layer from above the cap layer comprises ashing the photoresist layer from above the cap layer.

116. The method of claim 101, wherein performing a first anisotropic etching process into a region of the cap layer underlying the opening in the photoresist layer comprises performing a first anisotropic etching process by one of plasma etching and wet chemical etching into a region of the cap layer underlying the opening in the photoresist layer.

117. The method of claim 101, wherein performing a second anisotropic etching process comprises performing a second anisotropic etching process by plasma etching.

118. The method of claim 101, further comprising removing at least substantially all of the cap layer while performing the second anisotropic etching process.

119. The method of claim 101, further comprising:

thinning the cap layer while performing the second anisotropic etching process; and

thereafter, removing a remaining portion of the cap layer.

120. The method of claim 119, wherein removing a remaining portion of the cap layer comprises removing a remaining portion of the cap layer by a chemical mechanical polishing process.

121. The method of claim 101, wherein the structure layer comprises a semiconductor substrate.

122. The method of claim 101, wherein the structure layer comprises a layer of conductive material.

123. The method of claim 122, wherein the layer of conductive material comprises a patterned layer of conductive material.